



## 64K × 8 ELECTRICALLY ERASABLE EPROM

### **Table of Contents-**

|     |                                           |    |
|-----|-------------------------------------------|----|
| 1.  | GENERAL DESCRIPTION .....                 | 2  |
| 2.  | FEATURES .....                            | 2  |
| 3.  | PIN CONFIGURATIONS .....                  | 3  |
| 4.  | BLOCK DIAGRAM .....                       | 4  |
| 5.  | PIN DESCRIPTION.....                      | 4  |
| 6.  | FUNCTIONAL DESCRIPTION .....              | 5  |
| 7.  | TABLE OF OPERATING MODES .....            | 7  |
| 8.  | DC CHARACTERISTICS.....                   | 8  |
| 9.  | CAPACITANCE.....                          | 9  |
| 10. | AC CHARACTERISTICS .....                  | 9  |
| 11. | READ OPERATION DC CHARACTERISTICS .....   | 10 |
| 12. | READ OPERATION AC CHARACTERISTICS.....    | 10 |
| 13. | DC PROGRAMMING CHARACTERISTICS.....       | 11 |
| 14. | AC PROGRAMMING/ERASE CHARACTERISTICS..... | 12 |
| 15. | TIMING WAVEFORMS .....                    | 13 |
| 16. | SMART PROGRAMMING ALGORITHM 1.....        | 15 |
| 17. | SMART PROGRAMMING ALGORITHM 2.....        | 16 |
| 18. | SMART ERASE ALGORITHM .....               | 17 |
| 19. | ORDERING INFORMATION .....                | 18 |
| 20. | PACKAGE DIMENSIONS .....                  | 19 |
| 21. | VERSION HISTORY .....                     | 20 |



## 1. GENERAL DESCRIPTION

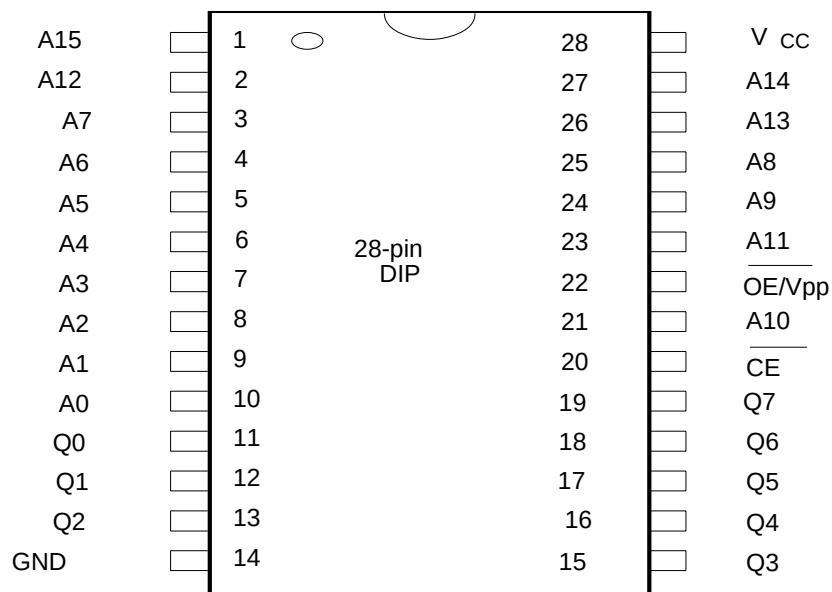
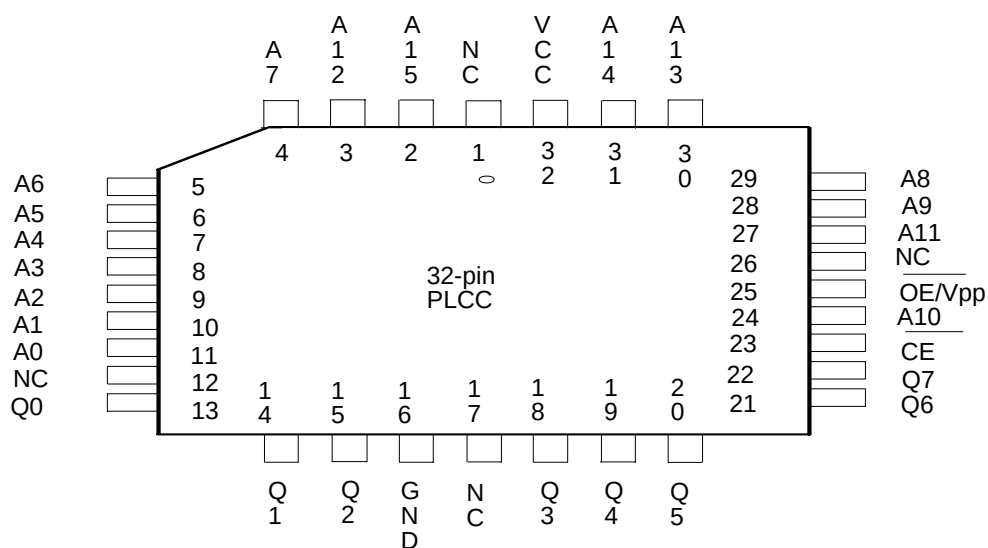
The W27C512 is a high speed, low power Electrically Erasable and Programmable Read Only Memory organized as  $65536 \times 8$  bits that operates on a single 5 volt power supply. The W27C512 provides an electrical chip erase function.

## 2. FEATURES

- High speed access time: 45/70/90/120 nS (max.)
- Read operating current: 30 mA (max.)
- Erase/Programming operating current: 30 mA (max.)
- Standby current: 1 mA (max.)
- Single 5V power supply
- +14V erase/+12V programming voltage
- Fully static operation
- All inputs and outputs directly TTL/CMOS compatible
- Three-state outputs
- Available packages: 28-pin 600 mil DIP, 330 mil 32-pin PLCC

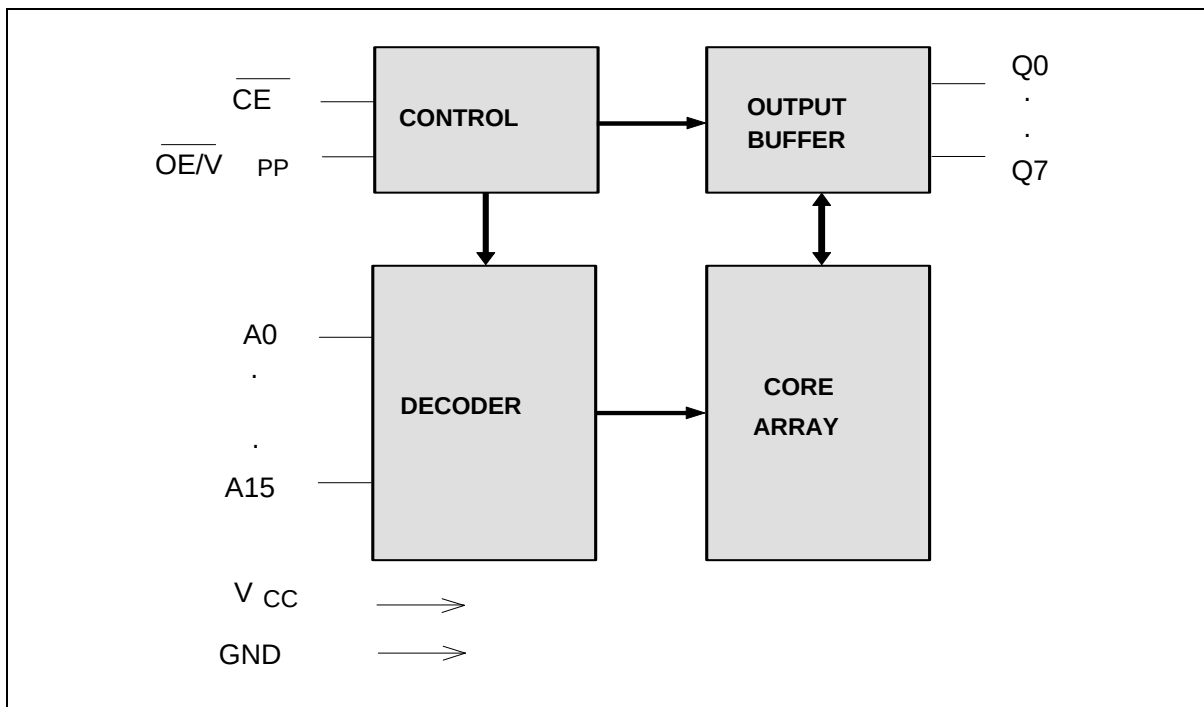


### 3. PIN CONFIGURATIONS





#### 4. BLOCK DIAGRAM



#### 5. PIN DESCRIPTION

| SYMBOL                 | DESCRIPTION                                 |
|------------------------|---------------------------------------------|
| A0–A15                 | Address Inputs                              |
| Q0–Q7                  | Data Inputs/Outputs                         |
| $\overline{CE}$        | Chip Enable                                 |
| $\overline{OE/V_{PP}}$ | Output Enable, Program/Erase Supply Voltage |
| $V_{CC}$               | Power Supply                                |
| GND                    | Ground                                      |
| NC                     | No Connection                               |



## 6. FUNCTIONAL DESCRIPTION

### Read Mode

Like conventional UVEPROMs, the W27C512 has two control functions, both of which produce data at the outputs.  $\overline{CE}$  is for power control and chip select.  $\overline{OE}/V_{PP}$  controls the output buffer to gate data to the output pins. When addresses are stable, the address access time ( $T_{ACC}$ ) is equal to the delay from  $\overline{CE}$  to output ( $T_{CE}$ ), and data are available at the outputs  $T_{OE}$  after the falling edge of  $\overline{OE}/V_{PP}$ , if  $T_{ACC}$  and  $T_{CE}$  timings are met.

### Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27C512 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

Erase mode is entered when  $\overline{OE}/V_{PP}$  is raised to  $V_{PE}$  (14V),  $V_{CC} = V_{CE}$  (5V),  $A_9 = V_{PE}$  (14V),  $A_0$  low, and all other address pins low and data input pins high. Pulsing  $\overline{CE}$  low starts the erase operation.

### Erase Verify Mode

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to "1" or not. The erase verify mode ensures a substantial erase margin if  $V_{CC} = V_{CE}$  (3.75V),  $\overline{CE}$  low, and  $\overline{OE}/V_{PP}$  low.

### Program Mode

Programming is performed exactly as it is in conventional UVEPROMs, and programming is the only way to change cell data from "1" to "0." The program mode is entered when  $\overline{OE}/V_{PP}$  is raised to  $V_{PP}$  (12V),  $V_{CC} = V_{CP}$  (5V), the address pins equal the desired addresses, and the input pins equal the desired inputs. Pulsing  $\overline{CE}$  low starts the programming operation.

### Program Verify Mode

All of the bytes in the chip must be verified to check whether they have been successfully programmed with the desired data or not. Hence, after each byte is programmed, a program verify operation should be performed. The program verify mode automatically ensures a substantial program margin. This mode will be entered after the program operation if  $\overline{OE}/V_{PP}$  low and  $\overline{CE}$  low.

### Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When  $\overline{CE}$  high, erasing or programming of non-target chips is inhibited, so that except for the  $\overline{CE}$  and  $\overline{OE}/V_{PP}$  pins, the W27C512 may have common inputs.

**Standby Mode**

The standby mode significantly reduces  $V_{CC}$  current. This mode is entered when  $\overline{CE}$  high. In standby mode, all outputs are in a high impedance state, independent of  $\overline{OE}/V_{PP}$ .

**Two-line Output Control**

Since EPROMs are often used in large memory arrays, the W27C512 provides two control inputs for multiple memory connections. Two-line control provides for lowest possible memory power dissipation and ensures that data bus contention will not occur.

**System Considerations**

An EPROM's power switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby current levels ( $I_{SB}$ ), active current levels ( $I_{CC}$ ), and transient current peaks produced by the falling and rising edges of  $\overline{CE}$ . Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1  $\mu$ F ceramic capacitor connected between its  $V_{CC}$  and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7  $\mu$ F electrolytic capacitor should be placed at the array's power supply connection between  $V_{CC}$  and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.



## 7. TABLE OF OPERATING MODES

(V<sub>PP</sub> = 12V, V<sub>PE</sub> = 14V, V<sub>HH</sub> = 12V, V<sub>CP</sub> = 5V, V<sub>CE</sub> = 5V, X = V<sub>IH</sub> or V<sub>IL</sub>)

| MODE                            | PINS                   |                            |                 |                 |                 |          |
|---------------------------------|------------------------|----------------------------|-----------------|-----------------|-----------------|----------|
|                                 | $\overline{\text{CE}}$ | $\overline{\text{OE/VPP}}$ | A0              | A9              | V <sub>CC</sub> | OUTPUTS  |
| Read                            | V <sub>IL</sub>        | V <sub>IL</sub>            | X               | X               | V <sub>CC</sub> | DOUT     |
| Output Disable                  | V <sub>IL</sub>        | V <sub>IH</sub>            | X               | X               | V <sub>CC</sub> | High Z   |
| Standby (TTL)                   | V <sub>IH</sub>        | X                          | X               | X               | V <sub>CC</sub> | High Z   |
| Standby (CMOS)                  | V <sub>CC</sub> ±0.3V  | X                          | X               | X               | V <sub>CC</sub> | High Z   |
| Program                         | V <sub>IL</sub>        | V <sub>PP</sub>            | X               | X               | V <sub>CP</sub> | DIN      |
| Program Verify                  | V <sub>IL</sub>        | V <sub>IL</sub>            | X               | X               | V <sub>CC</sub> | DOUT     |
| Program Inhibit                 | V <sub>IH</sub>        | V <sub>PP</sub>            | X               | X               | V <sub>CP</sub> | High Z   |
| Erase                           | V <sub>IL</sub>        | V <sub>PE</sub>            | V <sub>IL</sub> | V <sub>PE</sub> | V <sub>CE</sub> | DIH      |
| Erase Verify                    | V <sub>IL</sub>        | V <sub>IL</sub>            | X               | X               | 3.75            | DOUT     |
| Erase Inhibit                   | V <sub>IH</sub>        | V <sub>PE</sub>            | X               | X               | V <sub>CE</sub> | High Z   |
| Product Identifier-manufacturer | V <sub>IL</sub>        | V <sub>IL</sub>            | V <sub>IL</sub> | V <sub>HH</sub> | V <sub>CC</sub> | DA (Hex) |
| Product Identifier-device       | V <sub>IL</sub>        | V <sub>IL</sub>            | V <sub>IH</sub> | V <sub>HH</sub> | V <sub>CC</sub> | 08 (Hex) |



## 8. DC CHARACTERISTICS

### Absolute Maximum Ratings

| PARAMETER                                                                                  | RATING           | UNIT |
|--------------------------------------------------------------------------------------------|------------------|------|
| Operation Temperature                                                                      | 0 to +70         | °C   |
| Storage Temperature                                                                        | -65 to +125      | °C   |
| Voltage on all Pins with Respect to Ground Except $\overline{OE}/V_{PP}$ , A9 and VCC Pins | -0.5 to VCC +0.5 | V    |
| Voltage on $\overline{OE}/V_{PP}$ Pin with Respect to Ground                               | -0.5 to +14.5    | V    |
| Voltage on A9 Pin with Respect to Ground                                                   | -0.5 to +14.5    | V    |
| Voltage VCC Pin with Respect to Ground                                                     | -0.5 to +7       | V    |

**Note:** Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### DC Erase Characteristics

(TA = 25° C ±5° C, VCC = 5.0V ±5%)

| PARAMETER                         | SYM. | CONDITIONS                                                 | LIMITS |      |       | UNIT |
|-----------------------------------|------|------------------------------------------------------------|--------|------|-------|------|
|                                   |      |                                                            | MIN.   | TYP. | MAX.  |      |
| Input Load Current                | ILI  | VIN = VIL or VIH                                           | -10    | -    | 10    | μA   |
| VCC Erase Current                 | ICP  | $\overline{CE} = V_{IL}$ , $\overline{OE}/V_{PP} = V_{PE}$ | -      | -    | 30    | mA   |
| VPP Erase Current                 | IPP  | $\overline{CE} = V_{IL}$ , $\overline{OE}/V_{PP} = V_{PE}$ | -      | -    | 30    | mA   |
| Input Low Voltage                 | VIL  | -                                                          | -0.3   | -    | 0.8   | V    |
| Input High Voltage                | VIH  | -                                                          | 2.4    | -    | 5.5   | V    |
| Output Low Voltage (Verify)       | VOL  | IOL = 2.1 mA                                               | -      | -    | 0.45  | V    |
| Output High Voltage (Verify)      | VOH  | IOH = -0.4 mA                                              | 2.4    | -    | -     | -    |
| A9 Erase Voltage                  | VID  | -                                                          | 13.75  | 14   | 14.25 | V    |
| VPP Erase Voltage                 | VPE  | -                                                          | 13.75  | 14   | 14.25 | V    |
| VCC Supply Voltage (Erase)        | VCE  | -                                                          | 4.75   | 5.0  | 5.25  | V    |
| VCC Supply Voltage (Erase Verify) | VCE  | -                                                          | 3.5    | 3.75 | 4.0   | V    |

**Note:** VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.



## 9. CAPACITANCE

( $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $f = 1\text{ MHz}$ )

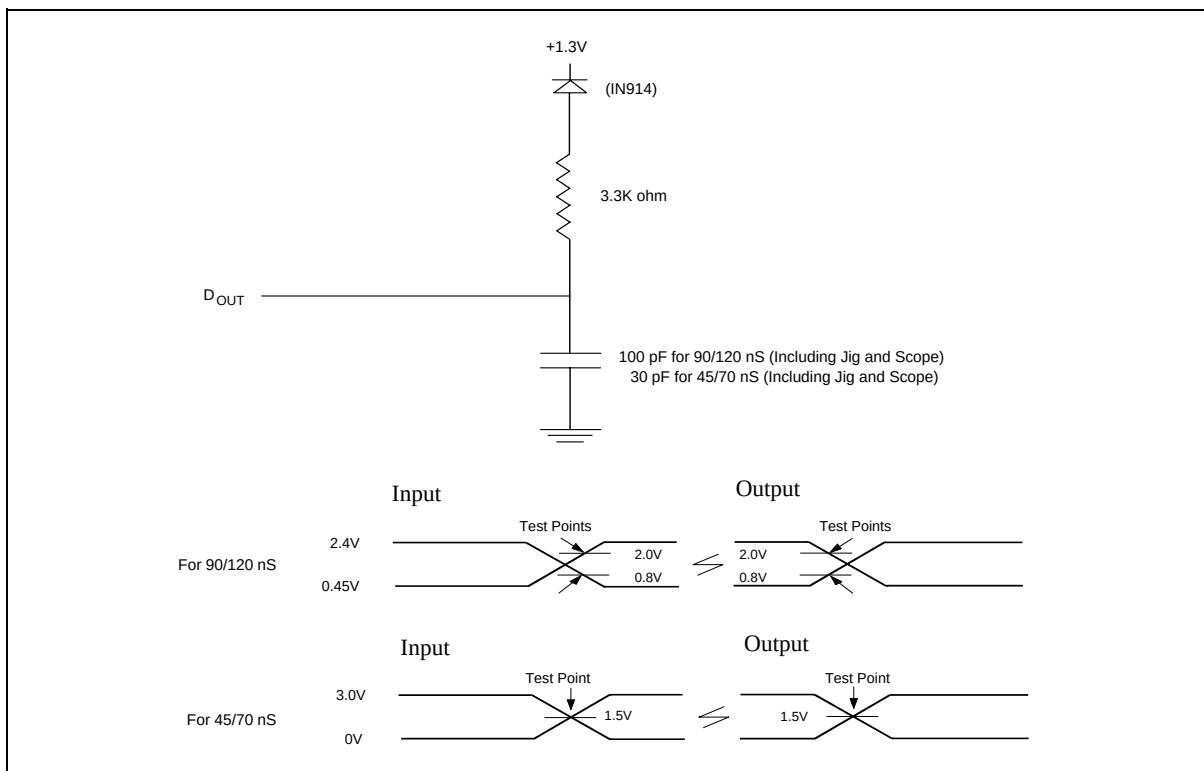
| PARAMETER          | SYMBOL           | CONDITIONS            | MAX. | UNIT |
|--------------------|------------------|-----------------------|------|------|
| Input Capacitance  | C <sub>IN</sub>  | V <sub>IN</sub> = 0V  | 6    | pF   |
| Output Capacitance | C <sub>OUT</sub> | V <sub>OUT</sub> = 0V | 12   | pF   |

## 10. AC CHARACTERISTICS

### AC Test Conditions

| PARAMETER                               | CONDITIONS                                                                   |                                                                               |
|-----------------------------------------|------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|                                         | 45/70 nS                                                                     | 90/120 nS                                                                     |
| Input Pulse Levels                      | 0 to 3.0V                                                                    | 0.45V to 2.4V                                                                 |
| Input Rise and Fall Times               | 5 nS                                                                         | 10 nS                                                                         |
| Input and Output Timing Reference Level | 1.5V/1.5V                                                                    | 0.8V/2.0V                                                                     |
| Output Load                             | C <sub>L</sub> = 30 pF,<br>I <sub>OH</sub> /I <sub>OL</sub> = -0.4 mA/2.1 mA | C <sub>L</sub> = 100 pF,<br>I <sub>OH</sub> /I <sub>OL</sub> = -0.4 mA/2.1 mA |

### AC Test Load and Waveforms





## 11. READ OPERATION DC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V ±5%, T<sub>A</sub> = 0 to 70° C)

| PARAMETER                                    | SYM.             | CONDITIONS                                                              | LIMITS |      |                       | UNIT |
|----------------------------------------------|------------------|-------------------------------------------------------------------------|--------|------|-----------------------|------|
|                                              |                  |                                                                         | MIN.   | TYP. | MAX.                  |      |
| Input Load Current                           | I <sub>LI</sub>  | V <sub>IN</sub> = 0V to V <sub>CC</sub>                                 | -5     | -    | 5                     | μA   |
| Output Leakage Current                       | I <sub>LO</sub>  | V <sub>OUT</sub> = 0V to V <sub>CC</sub>                                | -10    | -    | 10                    | μA   |
| Standby V <sub>CC</sub> Current (TTL input)  | I <sub>SB</sub>  | $\overline{CE}$ = V <sub>IH</sub>                                       | -      | -    | 1.0                   | mA   |
| Standby V <sub>CC</sub> Current (CMOS input) | I <sub>SB1</sub> | $\overline{CE}$ = V <sub>CC</sub> ±0.3V                                 | -      | 5    | 100                   | μA   |
| V <sub>CC</sub> Operating Current            | I <sub>CC</sub>  | $\overline{CE}$ = V <sub>IL</sub><br>I <sub>OUT</sub> = 0 mA, f = 5 MHz | -      | -    | 30                    | mA   |
| Input Low Voltage                            | V <sub>IL</sub>  | -                                                                       | -0.3   | -    | 0.8                   | V    |
| Input High Voltage                           | V <sub>IH</sub>  | -                                                                       | 2.2    | -    | V <sub>CC</sub> + 0.5 | V    |
| Output Low Voltage                           | V <sub>OL</sub>  | I <sub>OL</sub> = 2.1 mA                                                | -      | -    | 0.45                  | V    |
| Output High Voltage                          | V <sub>OH</sub>  | I <sub>OH</sub> = -0.4 mA                                               | 2.4    | -    | -                     | V    |

## 12. READ OPERATION AC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V ±5%, T<sub>A</sub> = 0 to 70° C)

| PARAMETER                                              | SYM.             | W27C512-45 |      | W27C512-70 |      | W27C512-90 |      | W27C512-12 |      | UNIT |
|--------------------------------------------------------|------------------|------------|------|------------|------|------------|------|------------|------|------|
|                                                        |                  | MIN.       | MAX. | MIN.       | MAX. | MIN.       | MAX. | MIN.       | MAX. |      |
| Read Cycle Time                                        | T <sub>RC</sub>  | 45         | -    | 70         | -    | 90         | -    | 120        | -    | nS   |
| Chip Enable Access Time                                | T <sub>CE</sub>  | -          | 45   | -          | 70   | -          | 90   | -          | 120  | nS   |
| Address Access Time                                    | T <sub>ACC</sub> | -          | 45   | -          | 70   | -          | 90   | -          | 120  | nS   |
| Output Enable Access Time                              | T <sub>OE</sub>  | -          | 20   | -          | 30   | -          | 40   | -          | 55   | nS   |
| $\overline{OE}$ /V <sub>PP</sub> High to High-Z Output | T <sub>DF</sub>  | -          | 20   | -          | 30   | -          | 30   | -          | 30   | nS   |
| Output Hold from Address Change                        | T <sub>OH</sub>  | 0          | -    | 0          | -    | 0          | -    | 0          | -    | nS   |

**Note:** V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.



### 13. DC PROGRAMMING CHARACTERISTICS

(VCC = 5.0V  $\pm$ 5%, TA = 25° C  $\pm$ 5° C)

| PARAMETER                    | SYM.            | CONDITIONS                                                      | LIMITS |      |       | UNIT    |
|------------------------------|-----------------|-----------------------------------------------------------------|--------|------|-------|---------|
|                              |                 |                                                                 | MIN.   | TYP. | MAX.  |         |
| Input Load Current           | ILI             | VIN = VIL or VIH                                                | -10    | -    | 10    | $\mu$ A |
| VCC Program Current          | ICP             | $\overline{CE} = V_{IL}$ ,<br>$\overline{OE} / V_{PP} = V_{PP}$ | -      | -    | 30    | mA      |
| VPP Program Current          | I <sub>PP</sub> | $\overline{CE} = V_{IL}$ ,<br>$\overline{OE} / V_{PP} = V_{PP}$ | -      | -    | 30    | mA      |
| Input Low Voltage            | VIL             | -                                                               | -0.3   | -    | 0.8   | V       |
| Input High Voltage           | VIH             | -                                                               | 2.4    | -    | 5.5   | V       |
| Output Low Voltage (Verify)  | VOL             | IOL = 2.1 mA                                                    | -      | -    | 0.45  | V       |
| Output High Voltage (Verify) | VOH             | IOH = -0.4 mA                                                   | 2.4    | -    | -     | V       |
| A9 Silicon I.D. Voltage      | VID             | -                                                               | 11.5   | 12.0 | 12.5  | V       |
| VPP Program Voltage          | VPP             | -                                                               | 11.75  | 12.0 | 12.25 | V       |
| VCC Supply Voltage (Program) | VCP             | -                                                               | 4.75   | 5.0  | 5.25  | V       |



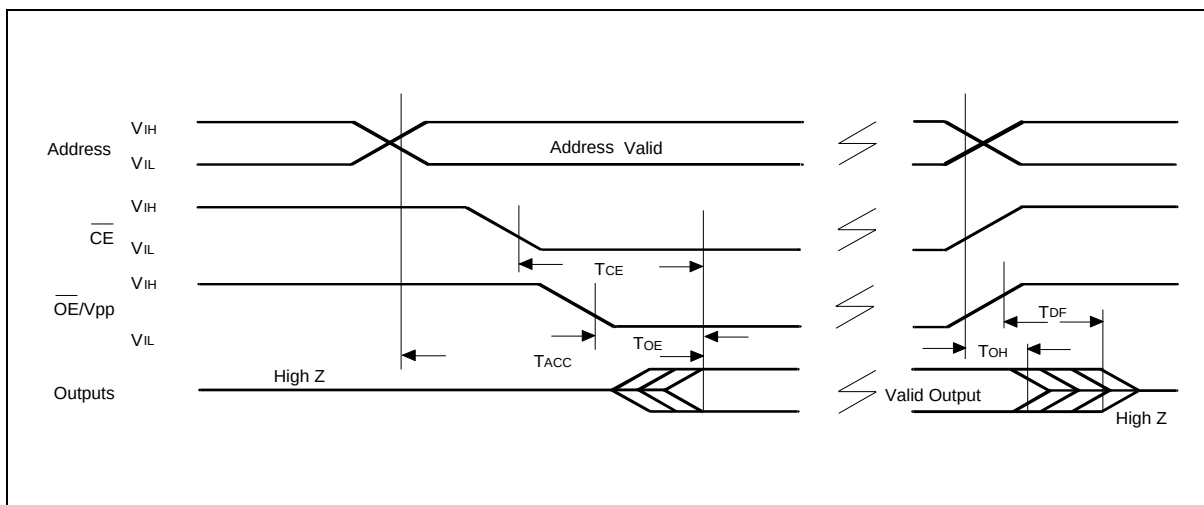
#### 14. AC PROGRAMMING/ERASE CHARACTERISTICS

(V<sub>CC</sub> = 5.0V ±5%, T<sub>A</sub> = 25° C ±5° C)

| PARAMETER                                                               | SYM.             | LIMITS |      |      | UNIT |
|-------------------------------------------------------------------------|------------------|--------|------|------|------|
|                                                                         |                  | MIN.   | TYP. | MAX. |      |
| $\overline{OE}$ /V <sub>PP</sub> Pulse Rise Time                        | TPRT             | 50     | -    | -    | nS   |
| Data Setup Time                                                         | T <sub>DS</sub>  | 2.0    | -    | -    | μS   |
| $\overline{CE}$ Program Pulse Width                                     | TPWP             | 95     | 100  | 105  | μS   |
| $\overline{CE}$ Erase Pulse Width                                       | TPWE             | 95     | 100  | 105  | mS   |
| Data Hold Time                                                          | T <sub>DH</sub>  | 2.0    | -    | -    | μS   |
| $\overline{OE}$ /V <sub>PP</sub> Setup Time                             | TOES             | 2.0    | -    | -    | μS   |
| $\overline{OE}$ /V <sub>PP</sub> Hold Time                              | TOEH             | 2.0    | -    | -    | μS   |
| Data Valid from $\overline{CE}$                                         | T <sub>DV1</sub> | 25     | -    | 1    | μS   |
| Data Valid from Address Change                                          | T <sub>DV2</sub> | 25     | -    | 1    | μS   |
| $\overline{CE}$ High to Output High Z                                   | T <sub>DFP</sub> | 0      | -    | 130  | nS   |
| Address Setup Time                                                      | T <sub>AS</sub>  | 2.0    | -    | -    | μS   |
| Address Hold Time                                                       | T <sub>AH</sub>  | 0      | -    | -    | μS   |
| Address Hold Time after $\overline{CE}$ High (Erase)                    | T <sub>AHC</sub> | 2.0    | -    | -    | μS   |
| $\overline{OE}$ /V <sub>PP</sub> Valid after $\overline{CE}$ High       | T <sub>VS</sub>  | 2.0    | -    | -    | μS   |
| $\overline{OE}$ /V <sub>PP</sub> Recovery Time                          | T <sub>VR</sub>  | 2.0    | -    | -    | μS   |
| Address Access Time During Erase Verify (V <sub>CC</sub> = 3.75V)       | T <sub>ACV</sub> | -      | -    | 250  | nS   |
| Output Enable Access Time during Erase Verify (V <sub>CC</sub> = 3.75V) | T <sub>OEV</sub> | -      | -    | 150  | nS   |

**Note:** V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.

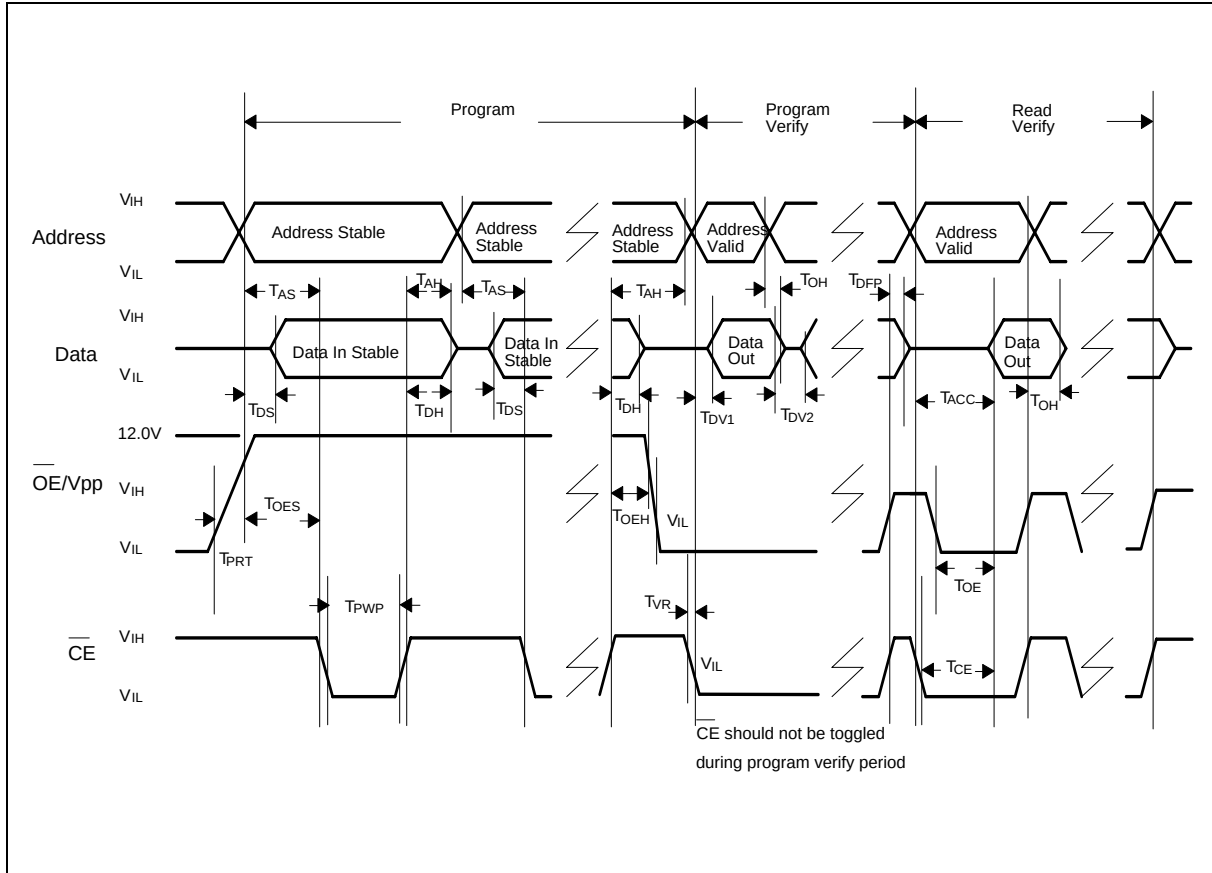
### AC Read Waveform

[illegible]



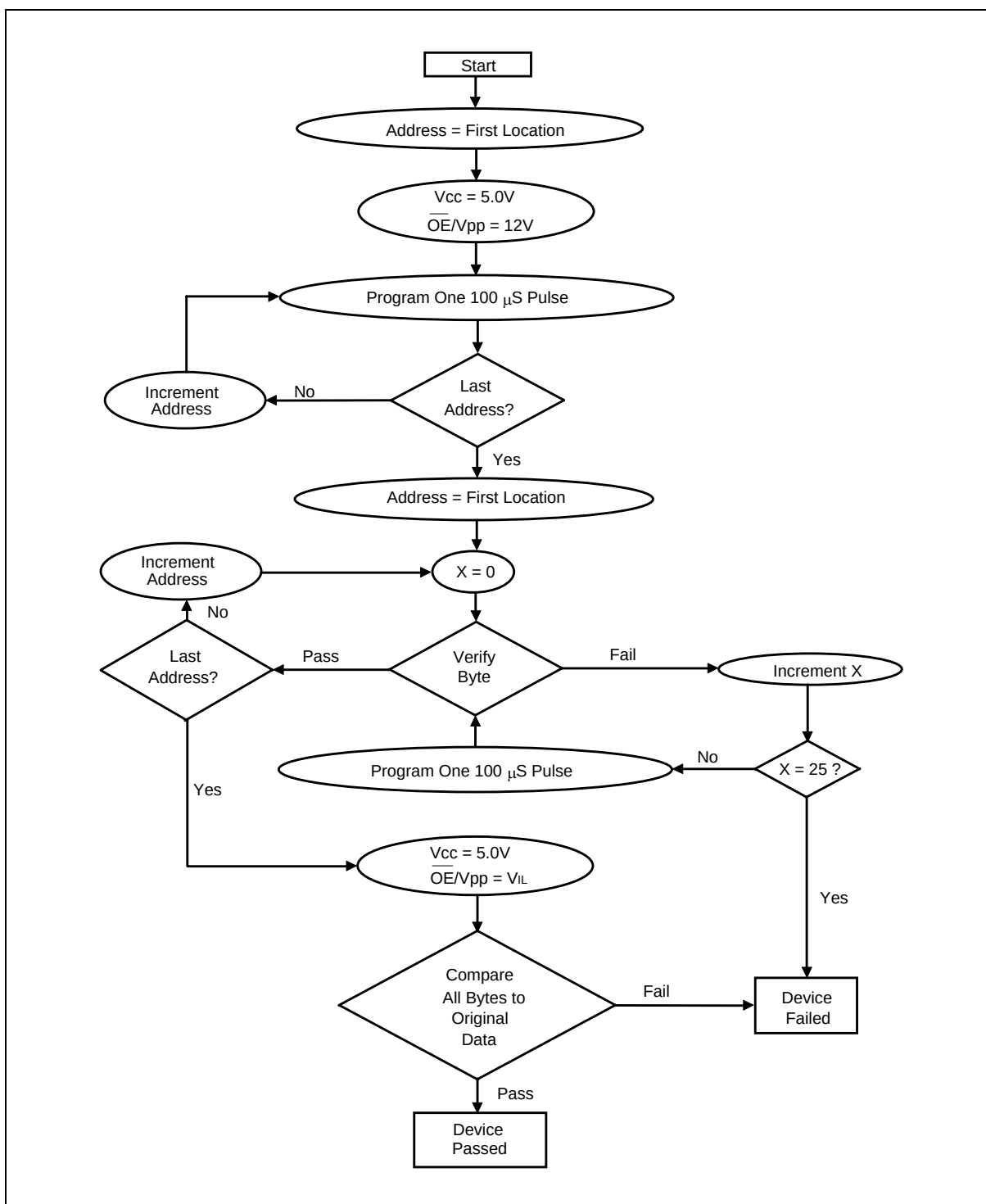
Timing Waveforms, continued

### Programming Waveform



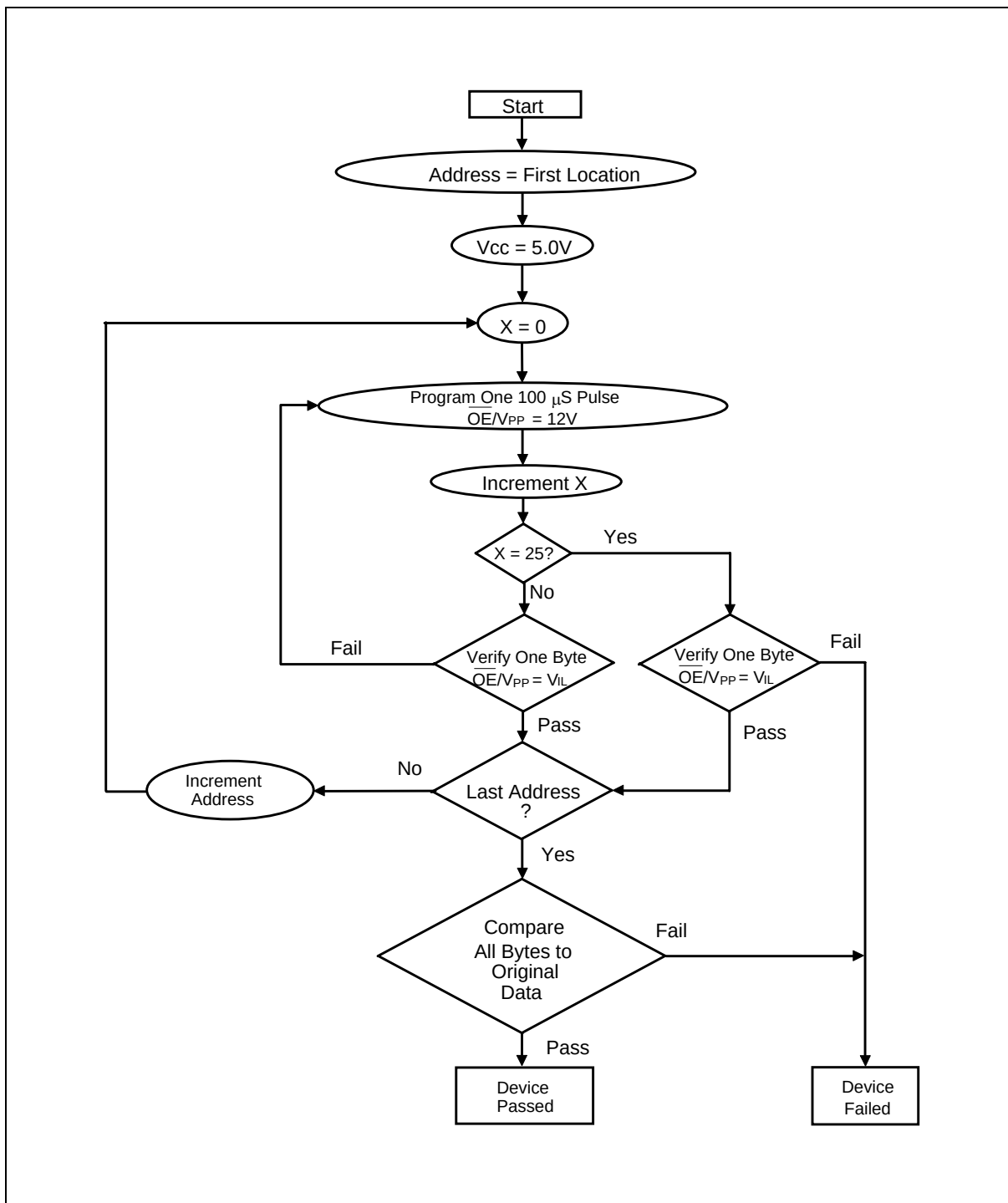


# 16. SMART PROGRAMMING ALGORITHM 1



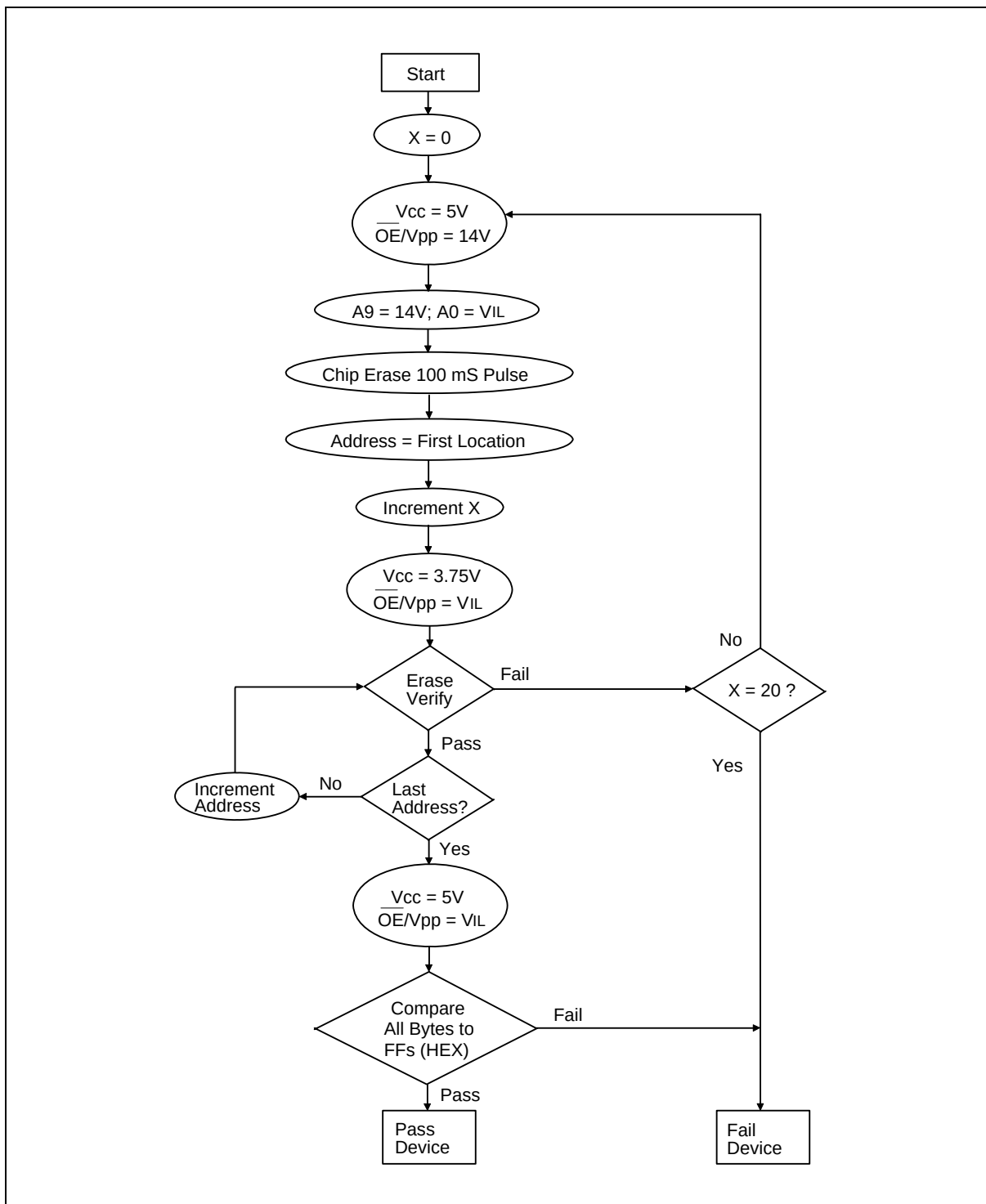


## 17. SMART PROGRAMMING ALGORITHM 2





## 18. SMART ERASE ALGORITHM





## 19. ORDERING INFORMATION

| PART NO.     | ACCESS<br>TIME<br>(nS) | OPERATING<br>CURRENT<br>MAX. (mA) | STANDBY<br>CURRENT<br>MAX. (μA) | PACKAGE               |
|--------------|------------------------|-----------------------------------|---------------------------------|-----------------------|
| W27C512-45   | 45                     | 30                                | 100                             | 600 mil DIP           |
| W27C512-70   | 70                     | 30                                | 100                             | 600 mil DIP           |
| W27C512-90   | 90                     | 30                                | 100                             | 600 mil DIP           |
| W27C512-12   | 120                    | 30                                | 100                             | 600 mil DIP           |
| W27C512P-45  | 45                     | 30                                | 100                             | 32-pin PLCC           |
| W27C512P-70  | 70                     | 30                                | 100                             | 32-pin PLCC           |
| W27C512P-90  | 90                     | 30                                | 100                             | 32-pin PLCC           |
| W27C512P-12  | 120                    | 30                                | 100                             | 32-pin PLCC           |
| W27C512-45Z  | 45                     | 30                                | 100                             | 600 mil DIP Lead Free |
| W27C512P-45Z | 45                     | 30                                | 100                             | 32-pin PLCC Lead Free |

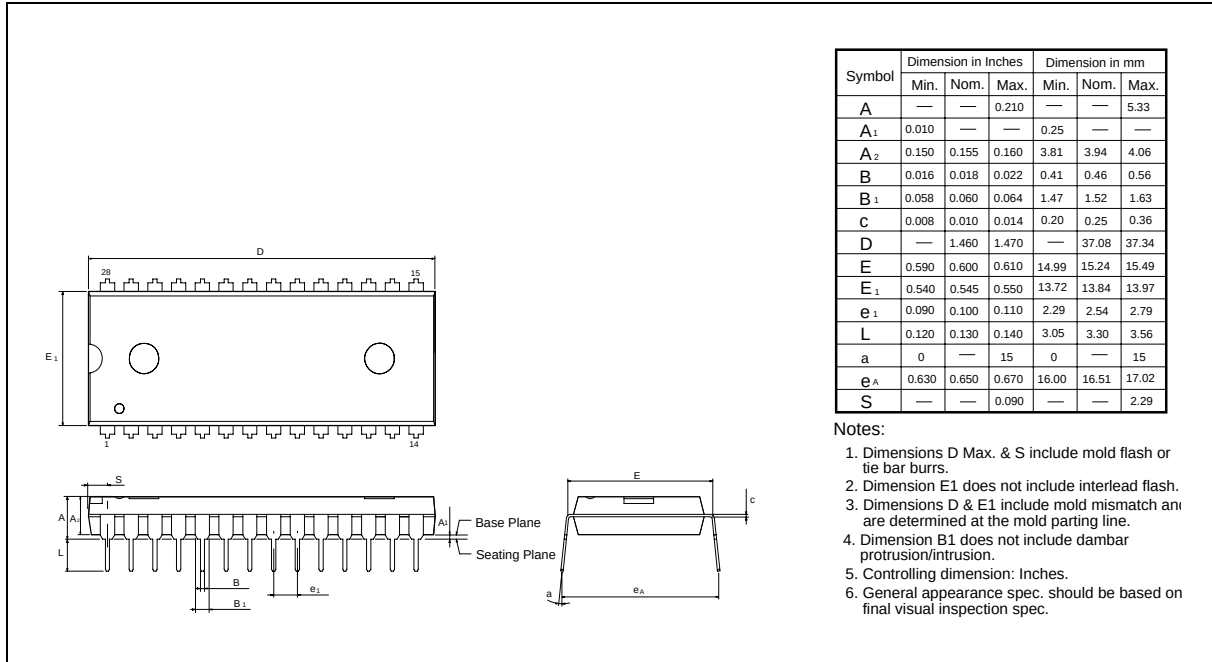
### Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

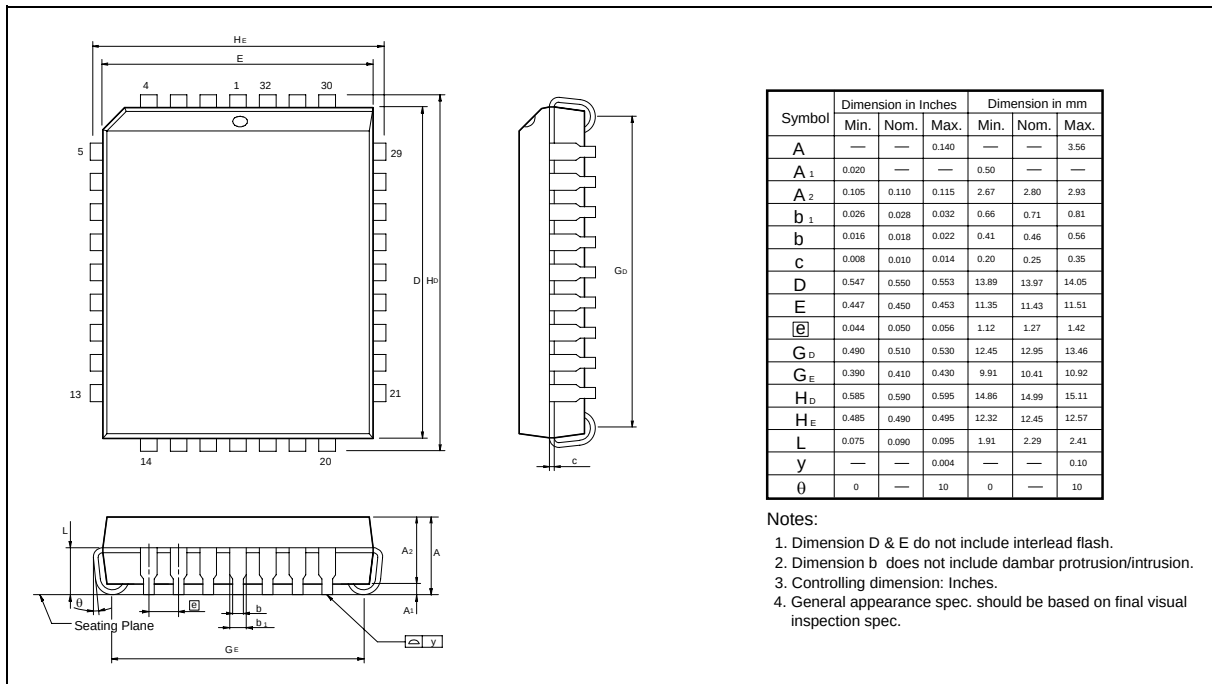


## 20. PACKAGE DIMENSIONS

### 28-pin P-DIP



### 32-pin PLCC





## 21. VERSION HISTORY

| VERSION | DATE           | PAGE        | DESCRIPTION                                                                                                   |
|---------|----------------|-------------|---------------------------------------------------------------------------------------------------------------|
| A1      | Mar. 1998      |             | Initial Issued                                                                                                |
| A2      | Sep. 1998      | 6           | Correct Input High Voltage ( $V_{IH}$ ) from 2.0 (min) to 2.2 (max)                                           |
|         |                | 4, 6        | Correct VCC from 5.0 $\pm 10\%$ to 5.0 $\pm 5\%$                                                              |
| A3      | Aug. 1999      | 1, 5, 6, 13 | Add 45 nS binning                                                                                             |
|         |                | 2, 3        | Modify function description ( $V_{IL}$ and $V_{IH}$ ):<br>$V_{IL} \rightarrow$ Low; $V_{IH} \rightarrow$ High |
| A4      | Nov. 1999      | 6           | Typo correction                                                                                               |
| A5      | April 14, 2005 | 15          | Adding important notice                                                                                       |
| A6      | Jan. 9, 2006   | 18          | Ordering Information: Add<br>W27C512-45Z and W27C512P-45Z Lead free part                                      |

### Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.